

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for improving hot carrier effects in complementary metal oxide semiconductor (CMOS) devices, the method comprising:
 - forming a first configuration of insulating material over a first group of the CMOS devices, said first group of the CMOS devices comprising NFET devices; and
 - forming a second configuration of insulating material over a second group of the CMOS devices, said second group of the CMOS devices comprises PFET devices;
 - wherein said first and said second configurations of insulating material are formed subsequent to a silicidation of the CMOS devices and prior to formation of a first interlevel (ILD) dielectric material over the CMOS devices; and
 - wherein said first configuration of insulating material comprises a tensile layer over said NFET devices and said second configuration of insulating material comprises a compressive layer over said PFET devices.
2. (currently amended) The method of claim 1, wherein said first configuration of insulating material further comprises at least a pair of individual insulating layers, and said second configuration of insulating devices-material further comprises a single insulating layer.
3. (cancelled)
4. (original) The method of claim 2, wherein said first group of the CMOS devices comprises gate oxide thicknesses of a first range and said second group of the CMOS devices comprises gate oxide thicknesses of a second range.
5. (original) The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises a second nitride layer.

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6. (original) The method of claim 5, wherein said first nitride layer is a tensile nitride layer, and said second nitride layer is a compressive nitride layer.

7. (original) The method of claim 6, wherein said first nitride layer is Si_3N_4 deposited using a BTBAS (Bis(TertiaryButylAmino)Silane) precursor, said second nitride layer is Si_3N_4 deposited by plasma enhanced chemical vapor deposition (PECVD) using a silane (SiH_2) precursor, and said oxide layer is tetrachethyl orthosilicate (TEOS).

8. (withdrawn) The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitride layer and a third nitride layer, and said single insulating layer further comprises a second nitride layer.

9. (withdrawn) The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises said first nitride layer.

10. (withdrawn) The method of claim 2, wherein said pair of individual insulating layers further comprises a first nitrido layer and a second nitride layer, and said single insulating layer further comprises said first nitride layer.

11. (withdrawn) The method of claim 1, wherein:

 said first configuration of insulating material further comprises one of a single nitride layer and a single oxide layer; and

 said second configuration of insulating material further comprises one of a single nitride layer, a single oxide layer, and a combination of a nitride and an oxide layer.

12. (withdrawn) The method of claim 1, wherein said first configuration of insulating material comprises a compressive material and said second configuration of insulating material comprises a tensile material.

13. (withdrawn) A structure for improving hot carrier effects in complementary metal oxide semiconductor (CMOS) devices, comprising:

a first configuration of insulating material formed over a first group of the CMOS devices; and

a second configuration of insulating material formed over a second group of the CMOS devices;

wherein said first and said second configurations of insulating material are formed subsequent to a silicidation of the CMOS devices and prior to formation of a first interlevel (ILD) dielectric material over the CMOS devices.

14. (withdrawn) The structure of claim 13, wherein said first configuration further comprises at least a pair of individual insulating layers, and said second configuration of insulating devices further comprises a single insulating layer.

15. (withdrawn) The structure of claim 14, wherein said first group of the CMOS devices comprises NFET devices and said second group of the CMOS devices comprises PFET devices.

16. (withdrawn) The structure of claim 14, wherein said first group of the CMOS devices comprises gate oxide thicknesses of a first range and said second group of the CMOS devices comprises gate oxide thicknesses of a second range.

17. (withdrawn) The structure of claim 14, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises a second nitride layer.

18. (original) The structure of claim 17, wherein said first nitride layer is a tensile nitride layer, and said second nitride layer is a compressive nitride layer.

19. (withdrawn) The structure of claim 18, wherein said first nitride layer is Si₃N₄ deposited using a BTBAS (Bis(TertiaryButylAmino)Silane) precursor, said second nitride layer is Si₃N₄ deposited by plasma enhanced chemical vapor deposition (PECVD) using a silane (SiH₂) precursor, and said oxide layer is tetraethyl orthosilicate (TEOS).

20. (withdrawn) The structure of claim 14, wherein said pair of individual insulating layers further comprises a first nitride layer and a third nitride layer, and said single insulating layer further comprises a second nitride layer.

21. (withdrawn) The structure of claim 14, wherein said pair of individual insulating layers further comprises a first nitride layer and an oxide layer, and said single insulating layer further comprises said first nitride layer.

22. (withdrawn) The structure of claim 12, wherein said pair of individual insulating layers further comprises a first nitride layer and a second nitride layer, and said single insulating layer further comprises said first nitride layer.

23. (withdrawn) The method of claim 13, wherein:

 said first configuration of insulating material further comprises one of a single nitride layer and a single oxide layer; and

 said second configuration of insulating material further comprises one of a single nitride layer, a single oxide layer, and a combination of a nitride and an oxide layer.

. 24. (withdrawn) The method of claim 13, wherein said first configuration of insulating material comprises a compressive material and said second configuration of insulating material comprises a tensile material.